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Application Number	10766761
Filing Date	2004-01-28
First Named Inventor	Craig Hampel
Art Unit	2611
Examiner Name	T. M. Wang
Attorney Docket Number	RBUS 1309-1US

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
/TW/	1	5541967		1996-07-30	Gluska et al.	
/TW/	2	6691214		2004-02-10	Li et al.	
/TW/	3	6735709		2004-05-11	Lee et al.	

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U.S.PATENT APPLICATION PUBLICATIONS

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/TW/	1	20020066001		2002-05-30	Olarig et al.	
/TW/	2	20020184461		2002-12-05	Zumkehr	
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/TW/	1	Supplementary EP Search Report for EP Patent Application 05711891.1-2415 mailed on 2007-12-18.	<input type="checkbox"/>

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Application Number	10/766,761														
Filing Date	28 January 2004														
First Named Inventor	Craig E. Hampel														
Group Art Unit	2637														
Examiner Name	Jayanti K. Patel														
Attorney Docket Number	RBUS 1309-1														
Sheet	2	of	2												

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/TW/	C1	EIA/JEDEC Standard No. 8-B (JESD8-B) "Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits," (Sept. 1999) 12 pages.	
/TW/	C2	EIA/JEDEC Standard No. 8-6 (EIA/JESD8-6) "High Speed Transceiver Logic (HSTL) A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits," (Aug. 1995) 16 pages.	
/TW/	C3	JEDEC Standard - JESD8-16 "Bus Interconnect Logic (BIC) for 1.2 Volts," (Apr. 2004) 16 pages.	
/TW/	C4	LEE, Ming-Ju Edward et al., "TP 15.3: A 90mW 4Gb/s Equalized I/O Circuit with Input Offset Cancellation" IEEE International Solid-State Circuits Conference, pages 252-253, Feb, 2000.	

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	Application Number	10/766,761		
	Filing Date	28 January 2004 (Herewith)		
	First Named Inventor	Craig E. Hampel		
	Group Art Unit			
	Examiner Name			
Sheet	1	of	4	Attorney Docket Number RBUS 1309-1

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.†	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code‡ (if known)			
/TW/	A1	4,384,354		Crawford et al.	05/17/1983	
/TW/	A2	5,122,978		Merrill	06/16/1992	
/TW/	A3	5,436,908		Fluker et al.	07/25/1995	
/TW/	A4	5,859,881		Ferraiolo et al.	01/12/1999	
/TW/	A5	6,047,346		Lau et al.	04/04/2000	
/TW/	A6	6,219,384		Kliza et al.	04/17/2001	
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/TW/	A13	6,469,555		Lau et al.	10/22/2002	
/TW/	A14	6,473,439		Zerbe et al.	10/29/2002	
/TW/	A15	6,510,503		Gillingham et al.	01/21/2003	
/TW/	A16	6,539,072		Donnelly et al.	03/25/2003	
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/TW/	A19	2003/0026399		Carlson	02/06/2003	

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Substitute for form 1448A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				C mplete If Known Application Number <u>10/766,761</u> Filing Date <u>28 January 2004 (Herewith)</u> First Named Inventor <u>Craig E. Hampel</u> Group Art Unit _____ Examiner Name _____ Attorney Docket Number <u>RBUS 1309-1</u>	
Sheet	<u>2</u>	of	<u>4</u>		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Application Number	10/766,761	
			Filing Date	28 January 2004 (Herewith)	
			First Named Inventor	Craig E. Hampel	
			Group Art Unit		
			Examiner Name		
Sheet	3	of	4	Attorney Docket Number	RBUS 1309-1

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/TW/	C1	PARIS, LLUIS ET AL, "WP 24.3 A 800MB/s 72Mb SDRAM with Digitally-Calibrated DLL," IEEE International Solid-State Circuits Conference (1999), 13 pages.	
/TW/	C2	NAKASE, YASUNOBU ET AL, "Source-Synchronization and Timing Vernier Techniques for 1.2-GB/s SDRAM Interface," IEEE Journal of Solid-State Circuits, Vol. 34, No. 4 (Apr. 1999), 494-501.	
/TW/	C3	GILLINGHAM, PETER, "SDRAM Architectural and Functional Overview," SDRAM Consortium (29 Aug 1997), 1-14.	
/TW/	C4	"Draft Standard for a High-Speed Memory Interface (SyncLink)", Draft 0.99 IEEE P1596.7-199X (1996), 56 pages	
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/TW/	C6	SDRAM Inc., "400 Mb/s/pin SDRAM," Draft Advance (9 Jul 1998), 1-69.	
/TW/	C7	ZERBE, JARED ET AL., U.S. Patent Application No. 09/776,550 filed 2 February 2001, entitled "Method and Apparatus for Evaluating and Calibrating a Signaling System."	
/TW/	C8	ZERBE, JARED ET AL., U.S. Patent Application No. 09/976,170 filed 21 October 2001, entitled "Method and Apparatus for Evaluating and Optimizing a Signaling System."	
/TW/	C9	RAMBUS "Direct Rambus Short Channel Layout Guide, Version 0.95" (August 2001), 40 pages	
/TW/	C10	RAMBUS "Direct Rambus Long Channel Design Guide" (2000), 45 pages	
/TW/	C11	RAMBUS, INC. "RDRAM Direct Rambus Clock Generator" (April 2002), 22 pages	

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		Examiner Name	
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/TW/	C13	REDWOOD TECHNOLOGY BRIEF "High Performance Parallel Bus Interface Technology", Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.	
/TW/	C14	LEWIS, DAVE, "Easy-to-Use LVDS Serdes for the Serdes Neophyte" National Semiconductor, (16 June 2003), pp. 1-5.	
/TW/	C15	INTEL "How to Measure RDRAM® System Clock Jitter" Application Note AP-667 (June 1999), pp. 1-15	

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